REMARKS

At the time the current Official Action was mailed, the Examiner rejected claims 1-41. Applicants have amended the numbering of claim 42 to be claim 41 to correct a clerical error in the numbering of the claims, and have added new claims 42-46. Further, Applicants have included an Election Under 37 C.F.R. §§ 3.71 and 3.73 and Power of Attorney, which is attached in Appendix A. Reconsideration of the application in view of the amendments and remarks set forth below is respectfully requested.

Rejections under 35 U.S.C. § 103

The Examiner rejected claims 1-41 under 35 U.S.C. § 103(a) as being unpatentable over Shieh et al. (U.S. Patent No. 6,003,118) in view of Keeth (U.S. Patent No. 6,016,282). In the rejection, the Examiner specifically stated:

> As to claim 1, Sheih substantially teaches the claimed method comprising the acts:
> a. providing a reference clock signal (external clock 22A) to a synchronization circuit (delay lock loop 22) coupled to an output data circuit (output buffer 24) configured to store the data being read from the memory device (DRAM Core 23) [figure 2.];
> b. delaying the reference clock signal by the synchronization circuit to produce a output clock signal [col. 4 lines 50-52];
> c. applying the output clock signal to the data output to remove the stored data therefrom synchronous with the reference clock signal [col. 1 lines 11-22].
>
> Shieh does not expressly disclose *distorting* the reference clock and apply the *distorted* output clock signal to remove the data. In summary, Shieh taught delaying but not distorting the reference clock signal to provide synchronization of outputting data.
>
> Keeth substantially teaches an adjustment circuit that distorts (adjusts the rising and falling edges of the clock signal) a reference clock signal (DCKL0) [col. 9 line 58-64].
>
> It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shieh by incorporating

> the adjustment circuit as taught by Keeth because both invention are directed toward data timing in memory environments. One would have made the modification because Keeth teaches that the adjustment circuit would compensate for duty cycle variations [col. 2 lines 46-55].
>
> ...
>
> As to claims 12-41, Shieh together with Keeth taught the claimed method of reducing duty cycle distortion therefore they also taught the claimed method of reading data from a memory device, the claimed processor based device, the claimed delay lock loop and the claimed integrated.
>
> Official Action, pages 2-5.

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

As a preliminary matter, it should be noted that *each claim* is independently patentably and must be addressed individually to properly account for the unique aspects recited therein. In the rejection, the Examiner only specifically addressed claims 1-11. For claims 12-41, the Examiner simply made a broad statement regarding the claims, but did not specifically address the subject matter recited in each of the claims. Because the Examiner did not specifically address claims 12-41, Applicants respectfully assert that the rejection of claims 12-41 is believed to be deficient in view of 37 C.F.R. § 1.104(c)(2). Applicants respectfully remind the Examiner of his duties and obligations under 37 C.F.R. § 1.104 and M.P.E.P. § 707.07 and request that the Examiner clarify his rejection and specifically cite the presently recited features in a future non-final Office Action. Accordingly, to further the prosecution of the present application, Applicants have addressed the specific rejection of independent claim 1.

The present application is directed to a technique for implementing a distorted duty cycle that compensates for data output of a memory device. In a memory device, such as a static dynamic random access memory (SDRAM) device or a double rate (DDR) SDRAM device, input and output latches hold information for and from the processor under the control (i.e., synchronous with) of the system clock. *See* Application, page 4, lines 1-15. As the data rates increase, distortion in the data output caused by switching components within the memory device becomes more significant. *See id.* at page 4, lines 17-21. For instance, with data being read on the rising and falling edges of the clock signal, the distortion of the duty cycle by the data latches may potentially result in a loss of data or the reading of incorrect data as the data rate increases. *See id.* at page 4, line 21- page 5 line 3. In accordance with embodiments of the present

technique, a course adjustment circuit 48 and two fine adjustment circuits 412 and 414 are utilized to distort the rising and falling edges of the CLKOUT signal to compensate for the duty cycle distortion in the latches. See *id.* at Fig. 6; page 19, line 5 - page 20, line 14. Further, the I/O model 420, which may include a copy of the data latch 208, models the behavior of the data latch 208 to provide the appropriate delays for the rising and falling edges of the clock. *See id.* at page 21, line 16 - page 22, line 21. Specifically, the output clock signal CLKOUT from the DLL is distorted in a phase inverse relationship to the distortion caused by the latch 208, such that the duty cycle distortion compensation for the output data signal results. Page 18, lines 9-11. To be clear, the present application discloses techniques to *distort* a reference clock signal and apply the *distorted clock signal* to clock the data from the data output circuit. Accordingly, claim 1 recites "delaying and distorting the reference clock cycle by the synchronization circuit to produce a distorted output clock signal" and "applying the distorted output clock signal to the data output circuit to remove the stored data therefrom synchronous with the reference clock signal."

In contrast, the Shieh reference discloses delay lock loop circuitry that is designed to reduce the locking period in a delay lock loop. *See* Shieh, col. 2, lines 40-44. In the reference, the clock signals are delayed for synchronization with the output data at the memory device output buffers. *See id.* at col. 1, lines 12-23. To achieve this synchronous access, the delay lock loop circuit includes a first path that has a first delay unit circuit for receiving an external clock signal and generating a delayed output clock signal. *See id.* at col. 3, line 30-35. Further, the delay lock circuit includes a second path that has a second delay unit circuit for generating a digital delay value during start-up of the memory system to pre-set the shift register circuit. *See*

id. at col. 3, lines 49-56. As such, the delay lock loop circuit is designed to reduce the initialization time of the DLL circuit lock state.

The Keeth reference describes vernier clock adjustment circuitry that compensates for the effects of duty cycle variation to accurately clock data in a memory device at higher data rate/transmission rates. *See* Keeth, col. 2, lines 46-55. The vernier adjustment circuits 66, 70, 74 and 60 permit read data from all DRAMS to arrive at a memory controller 22 within fixed, deterministic timing. *See id.* at col.7, lines 38-43. The vernier adjustment circuits 66, 70, 74 and 60 typically implement tapped delay lines to provide the required vernier adjustment delays. *See id.* at col. 7, lines 53-56. For instance, in the reference, the vernier adjustment circuits 70 and 74 provide delayed versions of the free running CCLK clock to respectively clock the write FIFO buffer 68 and the read FIFO buffer 72. *See id.* at col. 9 lines 11-16. The adjustments of the rising and falling edges of the CCLK clock provide a non-distorted clock signal to the write FIFO buffer 68 and the read FIFO buffer 70. *See id.* at col. 9, lines 3-16. To be clear, the Keeth reference discloses correcting a distorted signal to produce a non-distorted signal which is then used clock data from the buffers.

In the above-quoted rejection, the Examiner relied on the Shieh and Keeth references to reject claims 1-11. Specifically, the Examiner admitted that the Shieh reference does not expressly disclose *distorting* the reference clock and applying the distorted output clock signal to remove the data. In an attempt to cure this deficiency, the Examiner relied upon the Keeth reference to disclose distorting the clock signal. However, despite the Examiner's foregoing assertions, Applicants respectfully assert that the Shieh and Keeth references, alone or in

combination, at least fail to disclose "delaying and distorting the reference clock cycle by the synchronization circuit to produce a distorted output clock signal" and "applying the distorted output clock signal to the data output circuit to remove the stored data therefrom synchronous with the reference clock signal," as recited in claim 1. Accordingly, Applicants respectfully submit that the Examiner's attempts to cure the deficiencies of the Shieh reference are insufficient to establish a *prima facie* case of obviousness, as discussed below.

To begin, the Shieh and Keeth references, alone or in combination, do not disclose "delaying and distorting the reference clock cycle by the synchronization circuit to produce a distorted output clock signal" and "applying the distorted output clock signal to the data output circuit to remove the stored data therefrom synchronous with the reference clock signal," as recited in claim 1. As noted above, the Examiner admitted that the Shieh reference does not expressly disclose distorting the reference clock and applying the distorted output clock signal to remove the data. Indeed, the Shieh reference is silent with regard to the duty cycle of the clock signal and simply delays the signal to be synchronized with the data. Accordingly, the Shieh reference does not disclose the claimed subject matter.

Contrary to the Examiner's assertions noted above, Applicants respectfully assert that at best, the Keeth reference discloses that vernier clock adjustment circuitry adjusts the clock signal to remove distortion from the clock signal to produce a non-distorted clock signal which is used to clock data. In the Keeth reference, the vernier adjustment circuitry is utilized to permit the read and write data to arrive within a fixed deterministic timing period. *See* Keeth col. 7, lines 38-43. Further, the vernier adjustment circuitry is utilized to compensate for problems, such as

non-ideal waveforms. For instance, the ideal signal waveform is shown in Fig. 8A, which is a non-distorted waveform, while a non-ideal waveform is shown in FIG. 8B. *See id.* at Figs. 8A and 8B; col. 9, lines 47-57. Accordingly, the Keeth reference describes that the vernier adjustment circuitry compensates for the non-ideal waveform by adjusting the rising and falling edges to produce the ideal waveform. *See id.* at col. 9, lines 58-64. Essentially, this technique is *opposite* to the techniques recited in the present claims. Clearly, the Keeth reference does not disclose or suggest *distorting* the reference clock cycle to produce a distorted output clock signal, much less, apply the *distorted output clock signal* to the data output circuit to remove the stored data synchronously with the reference clock signal, as recited in the present claims. To the contrary, the Keeth reference discloses correcting the distortions in a reference clock signal and using the non-distorted signal to clock data. Accordingly, the Keeth reference not only fails to cure the deficiencies of the Shieh reference, but it actually teaches away from the claimed invention.

For at least the reasons set forth above, it is clear that the Shieh and Keeth references fail to disclose all the recited features of the instant claims, and thus cannot possibly render the claimed subject matter obvious. Accordingly, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 1-41.

New Claims

New claims 42-46 have been added by this response. Claims 42-46 are fully supported by the specification and add no new matter. In addition, claims 42-46 are believed allowable over the cited references for at least the reasons cited above. Accordingly, Applicants

respectfully request that the Examiner consider these new claims in view of the remarks set forth above.

Conclusion

In view of the remarks set forth above, Applicants respectfully request reconsideration of the Examiner's rejections and allowance of all pending claims 1-41 and new claims 42-46. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Fees Due with the Present Response

Applicants hereby request a one-month extension in the shortened statutory period for response to the Official Action from July 6, 2004 to August 6, 2004 in accordance with 37 C.F.R. § 1.136. The Commissioner is authorized to charge the requisite fee of $110.00 for the extension to the assignee's deposit account number 13-3092; Order No. MICS:0070/FLE 00-0917.

Further, Applicants have included one additional independent claim and four dependent claims with the present response. Applicants believe that the fees due for the addition of new claims 42-46 should be $176.00. Accordingly, Applicants hereby authorize the Commissioner to charge the requisite fee of $176.00 for the new claims to the assignee's deposit account number 13-3092; Order No. MICS:0070/FLE 00-0917. If this calculation has been made in error, Applicants hereby authorize the Commissioner to charge the appropriate fee to the above-referenced Deposit Account.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefor. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MICS:0070/FLE (00-0917).

Respectfully submitted,

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